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Single Event Effects Test Results and Their Applications to Spacecraft Electronics

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Single event effects test results for 37 typical devices used in satellite systems are presented. The data demonstrate that most standard and radiation hardened linear devices such as operational amplifiers, voltage references, voltage regulators, comparators, pulse-width modulators, and frequency synthesizers are susceptible to heavy-ion-induced effects. The severity of these effects varies for different devices and includes both upset and latchup. For a specific device, the probability of effects occurring is a nonlinear function of the transient amplitude, such that higher amplitude transients are much less likely to occur. Such effects can have very serious implications for space electronics. However, in most cases, these effects can be mitigated by simple techniques such as passive filtering, voting, appropriate parts selection, and, in case of pulse-width modulators, disabling of the internal soft start circuitry.

Nomenclature

$\mathrm{LET}_{0.25}$ = linear energy transfer, MeV · cm^2/mg at 25% of σ
R = upset rate per device, per day
σ = saturation cross section, cm^2

Introduction

BECAUSE of the increased level of integration of semiconductor devices and the increasing size of spacecraft, single event effects (SEE) phenomena have a significant impact on spacecraft electronic design and performance. SEE include potentially destructive single effects latchup (SEL), single event upsets (SEU) of digital registers, and single effects transients (SET) typically associated with operational amplifiers, voltage regulators, and references. These effects can cause on-orbit spacecraft spurious shutoffs, loss of communication traffic, or, in extreme cases, loss of the mission. In this paper we present test data, in the context of a spacecraft-level mitigation methodology, that can be used to mitigate the SEE effects. In particular, SEE data are presented for 37 operational amplifiers, comparators, voltage references, voltage regulators, pulse-width modulators, frequency synthesizers, rf amplifiers, transistors, clock drivers, and inverted AND (NAND) gates from various device manufacturers.

SEE Analysis Methodology and Test Data

Table 1 specifies the SEE that are of interest to circuit designers and need to be addressed as part of their worst-case circuit analysis to ensure that the circuit is immune to these effects.[1–9] As a first step in performing SEE analysis, a computer circuit simulation is performed to determine the SEE impact on the box performance as a result of an effect of each of the piece parts. In some cases, it is not practical and is cost prohibitive to eliminate completely the possibility of the effects that could cause electronics malfunctions. In this case, a tradeoff assessment is performed. During the assessment, the probability of the effect is traded off against the severity of the impact of such an effect on the spacecraft performance.

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For example, the SEE rate for a specific application can be estimated using the Peterson figure of merit (Refs. 1–3). The upset rate per device per day is given by

$$R = 200(\sigma)/(\mathrm{LET}_{0.25})^2 \tag{1}$$

In our experience, this expression is in relatively good agreement with on-orbit performance averaged over a spacecraft life of 10–15 years. More detailed analysis can be performed using the CREME computer program to predict upset rates more accurately when the analytical method indicates that a potential problem might exist.[9] In general, CREME calculations are in good agreement with the Peterson figure of merit provided that the CREME results are averaged other solar maximum and solar minimum periods (excluding solar proton events).

Finally, SEE testing of components for which no test data are available is needed. In this case, all testing was done at the Brookhaven National Laboratory Tandem Van de Graaff Facility. During the tests the devices were exposed to Li, Si, Cl, Fe, Ni, Br, and Au as shown in Table 2. These ions were selected to cover a wide range of test energies and linear energy transfers (LETs) and to simulate as best as practical the space environment. The accuracy of the environment simulation is limited by the ion energies and the corresponding range being lower than in space. However, for the majority of the tested devices, the range of ions (including Br and Au) used in a test is sufficient to penetrate into the devices' sensitive regions to simulate the effects of space ions on these devices.

SEE Test Results

Operational Amplifiers, Comparators, and Voltage References

Tables 3–5 provide the summary of the test data for operational amplifiers, comparators, and voltage references. The operational amplifiers and comparators were tested with the wide range of input bias voltages that covered device's operating range. Their outputs were terminated into high impedance resistive loads. If the circuit utilizing the device is designed to be immune to such transients it will be immune to SEE for both geosynchronous Earth orbit (GEO) and low Earth orbit (LEO). The probability of occurrence of such worst-case transients is low. This, when combined with information on the worst-case transient amplitude, is used to develop filtering requirements to make the circuit immune to their effects. Devices that were shown to be immune to Au ions are not expected to latchup in either GEO or LEO environments. Devices that are susceptible to latchup with Au or Ag ions have very low probability of latchup (one event in several thousand years). However, if the spacecraft is utilizing a large number of such devices the likelihood of latchup

Table 1 SEE on devices

Device	Effect
OP-amps	Rail-to-rail for duration of up to 15 μs. Upset rate depends on input and bias voltage.
Comparators	Rail-to-rail, 5 μs. Upset rate depends on input and bias voltage.
Voltage regulators/ref	Transients with rail-to-rail amplitude and 10-μs duration.
PWMs	Double pulses, two missing pulses, multiple missing pulses in a row, device shutoff. Assess impact in specific application.
Digital-to-analog	Transients of 50 mV, 5 V in amplitude for one clock cycle. Upset rate depends on amplitude of transients.
Application-specific integrated circuits (ASIC)	Upsets/errors/transients. Assess impact in specific application.
Phase lock loops (PLL)	Transients and permanent changes in output voltage. In synthesizer circuits can cause phase, amplitude, and frequency transients with duration determined by loop response.
Latches/shift registers	Upsets/errors/latchups. Assess impact in specific flip-flops, etc., application, transients, 5V, 50–100 ns.
Power MOSFETs (metal-oxide-semiconductor field effect transistors)	Operating voltage for non-SEE hard devices is 33% and for SEE hard devices is 80% of rated breakdown to avoid burnout and gate rupture with Vgs (off) > 5 V. (Vgs = gate-to-source voltage in volts.)
Opto-couplers	Susceptible to SET, 5 V transients with duration of 100 ns.
Field effect transistor (FET) drivers	$\pm$2.5 V, 150 ns output transients.
Analog switch	Momentary (15 μs) change in the state of the switch. Each switch can change state independently or simultaneously in pairs (S1 with S3 or S2 with S4). Rail-to-rail 15 μs transients at the outputs of any of the switches. Wrong switch input will momentarily gets connected to the wrong output (for example, if S2 momentarily gets connected to D3).

Table 2 Ion energies and LETs

Ion	Max energy, MeV	Range in Si, μm	LET in Si, MeV $\cdot$ cm^2/mg
Li	58	404	0.365
Si	203	85.8	7.51
Cl	224	68.8	11.1
Fe	270	43.7	24.1
Ni	280	44.6	26.2
Br	305	39.0	36.8
Au	390	30.5	83.9

increases proportionally to the number of devices. SEE effects for this class of devices typically include SET and SEL. The following key points can be deduced from the test results:

1) Duration of transients for comparators is <5 μs.

2) Duration of transients for slower operational amplifiers (op-amps) such as PM108, LM108, and LM158 is <15 μs.

3) Duration of transients for fast op-amps such as OP27, OP37, OP42, and OP270 series is <2 μs.

4) Worst-case transients for all devices are less than or equal to rail-to-rail voltage.

Input bias voltage does not have a significant impact on the upset rate of operational amplifiers, but it does impact SEU sensitivity of the comparators. Very few of the devices are susceptible to permanent damage.

The worst-case upset rates R for operational amplifiers, comparators, and voltage references are shown in Table 6. The worst-case voltage transients and duration as a function of output capacitance typical for voltage references are shown in Table 7.

Voltage Regulators

Two voltage regulators (LM117 and RH117) were tested (Table 8). The results support the following generalized guidelines for voltage regulators:

1) There is no substantial difference in SEE performance between RH and LM-type voltage regulators.

2) The average upset rate is $R = 3.1$ upsets/device/year ($L_{25\%} = 7.5$ MeVcm^2/mg, $\sigma = 2.4 \times 10^{-3}$).

3) The devices were tested with input voltages from 8 to 15 V and output voltage varying from 5 to 12 V. These voltage variations have minimal impact on SET performance.

4) Varying load resistance/load current has minimal impact on SET or the shape of transients. In our tests we varied load current from 35 to 200 mA.

5) Varying capacitance at the input of the device has no impact on SET performance. In our tests, we varied the input capacitance from 0.1 to 1 μF.

6) Capacitance at the device output (C_{out}) has significant impact on the shape of the output transients. With $C_{\text{out}} = 2$ μF, the worst-case transient is $V = \pm 0.5$ V, and duration $T = 80$ μs.

7) The transient amplitude is inversely proportional to square root of the increase in capacitance, or $V(\text{transient}) = 0.5 \times (2\ \mu\text{F}/C_{\text{out}})^{1/2}$ V. In other words, an increase in output capacitance from 2 to 16 μF causes an approximately factor of three decease in transient amplitude. This rule was verified over the C_{out} range from 2 to 160 μF.

8) The duration of the output transients, on the other hand, is proportional to square root of the increase in capacitance, or $T(\text{transient}) = 80 \times (C_{\text{out}}/2\ \mu\text{F})^{1/2}$ μs. In other words, an increase in output capacitance from 2 to 16 μF causes an approximately factor of three increase in transient duration. This rule was verified over the C_{out} range from 2 to 160 μF.

9) Finally, for $C_{\text{out}} = 0$ μF, the worst-case output transients were approximately $V = +2.0/-2.5$ V, with duration $T = 4$ μs.

Pulse-Width Modulators

The six pulse-width modulators (PWMs) (UC1864, UC1803, UC1825, SG1825, SG1525, and UC 1705) were tested (Table 9). SEEs on these devices include one missing output pulse, double pulse, multiple missing pulses, and destructive failures. The general conclusions were as follows:

1) The following PWMs are least susceptible to SEU: UC1825, SG1825, SG1525, and SG1843.

2) The UC1864 devices are immune to output dropouts provided the soft start pin is grounded.

3) UC1846 and UC1843 are susceptible to soft-start-induced output dropouts, but they have a low upset rate.

4) UC1825A and UC1803 are highly susceptible to SEU.

5) UC1803 is susceptible to failures.

Frequency Synthesizer Circuits

Five frequency synthesizers (LM2315, SP8858, SP8855, 3261, and 3282A) were tested (Table 10). SEEs on these devices include SEU of digital registers and momentary transient shifts in output frequencies. The general results were as follows:

1) Out of five synthesizer devices, LM2315 or 3282A are least susceptible to SEU.

2) The SP8855 device has the second lowest SEU rate.

3) SP8858 and Qualcomm devices are highly susceptible to SEU.

The impact of the spurious frequency transients on the system performance has to be evaluated against specific design and program requirements.

Digital and RF Devices

Two digital and two rf devices (54AC2525, SN54S30N, AC936, and 2NE356) were tested (Table 11). The general results were as follows:

1) Based on the limited test data, rf amplifiers and rf transistors are not susceptible to SEE.

Table 3 Summary of SEU data for operational amplifiers

Device	Vendor	Worst-case positive transients, V	Worst-case negative transients, V	Typical transients, V	Duration, μs	GEO upset rate/year for all transients >0.2 V	>1 V	>4 V	Latchup (Au, LET = 83.9)	Vcc
LM108	National	0.8	0.60	±0.3	15	12	0	0	No	±15
LM158	National	3.0	8.00	±0.5	10	1.5	8.5×10^{-2}	2.4×10^{-3}	No	
OP27A	Analog devices (AD)	1.0	8.00	0.6/−2.0	1	0.2	5.4×10^{-2}	3.1×10^{-4}	Damage at Au (LET = 83.9)	+15/−15
OP37	AD	3.0	4.00	2.0/−2.0	1	0.4	4.2×10^{-2}	1.6×10^{-4}	Damage at Ag (LET = 52.7)	±15
OP42	AD	10.0	17.0	2.0/2.0	2	10.2	8.8×10^{-3}	3.8×10^{-3}	No	±15
PM108	PMI	2.3	1.4	±0.3	15	8.7	——	0	No	+21/0
OP270	AD	1.5	1.6	±0.3	0.5	1.8	9.3×10^{-4}	0	No	+15/0
OP467	AD	+Rail	−Rail	±2	200 ns	1.1	1.6×10^{-2}	——	No	±5
OP470[a]	AD	——	——	——	——	——	——	——	83.9	±15
AMP01	AD	——	——	——	——	——	——	——	83.9	16.3/−15.4
RH1011	LT	——	——	——	——	——	——	——	No	±15
HS-390RH	AD	——	——	——	——	——	——	——	No	5/0
HS-22620RH	Harris	4	12	2/−3.5	0.5	——	0.1	——	No	±15
HS1135RH	Harris	2.5	2.5	——	50 ns	6.5×10^{-2}	——	——	No	+5.2/−5.4

[a] Tested only at LET = 83.9 MeVcm^2/mg.

Table 4 Summary of SEU data for comparators

Device	Vendor	Worst-case positive transients, V	Worst-case negative transients, V	Typical transients, V	Duration, μs	GEO upset rate/year for all transients >0.2 V	>1 V	>4 V	Latchup (Au, LET = 83.9)	Vcc
LM193	National	2.7	15.0	——	2	9.6	see LM139	see LM139	No	+15/0
LM139[a]	National	5	15	2/15	5	0.5	0.3	0.3	No	+15/0
LM139[b]	National	5	15	2/15	5	0.2	1.3×10^{-3}	0	No	+15/0
CMP01	AD	N/A	4.3	0.7	2	0.2	2.3×10^{-2}	4.3×10^{-3}	No	+5/0
LT1018[c]	Linear Tech (LT)	N/A	8	1.5	15	1.9	0.1	1.2×10^{-2}	No	+12/0
HS-139RH	Harris	10	12	±7	5	——	——	0.2	No	+12/0

[a] Differential input $\Delta V = 300$ mV. [b] Differential input $\Delta V = 2$ V. [c] Input bias voltage is 300 mV.

Table 5 Summary of SEU data for voltage references

Device	Vendor	Worst-case positive transients, V	Worst-case negative transients, V	Typical transients, V	Duration, μs	GEO upset rate/year for all transients >0.2 V	>1 V	>4 V	Latchup (Au, LET = 83.9)	Vcc
RH1009[a]	LT	0.15	0.4	0.1/0.3	20	0.7	0	0	No	15
RH1009[b]	LT	0.8	2	0.2/0.5	1	1.7	1.1×10^{-3}	0	No	15
RH1021[c]	LT	1	1.3	0.5/0.3	20	3.1×10^{-2}	not available	0	No	15
RH1021[d]	LT	3	6	0.5/0.8	5	0.1	2.5×10^{-2}	not available	No	15
RH1021[e]	LT	0.6	0.6	0.15/0.15	150	not available	0	0	No	15
AD584[f]	AD	1	1	——	10	——	——	0	No	12

[a] Includes 0.1-μF output cap.
[b] No output capacitor.
[c] Includes 0.1-μF output cap, $V_{in} = 15$ V through 511 Ω.
[d] No output capacitor, $V_{in} = 15$ V through 511 Ω.
[e] Includes 1.1-μF output cap, $V_{in} = 15$ V through 511 Ω.
[f] Includes 0.01-μF output cap and 100 Ω resistor on input voltage line.

Table 6 Worst-case upset rates for operational amplifiers, comparators, and voltage references

Transient size	Upsets/device/year
>200 mV	$R < 10$
>1 V	$R < 1$
>3–4 V	$R < 0.01$

Table 7 Worst-case voltage transients and duration as a function of output capacitance typical for voltage references

Output capacitor value, μF	Positive transients	Negative transients	Duration, μs
No output capacitor	40% of V_{out}	100% of V_{out}	<5
0.01	40% of V_{out}	40% of V_{out}	<10
0.1	20% of V_{out}	20% of V_{out}	<20
1.1	2% of V_{out}	2% of V_{out}	<150

Table 8 Summary of data for voltage references

Device	Vendor	Worst-case positive transients, V	Worst-case negative transients, V	Typical transients, V	Duration, μs	GEO upset rate/year for all transients >0.2 V	>1 V	>4 V	Latchup (Au, LET = 83.9)	Vcc
RH117[a]	LT	0.6	0.6	——	80	3.1	0	0	No	8
LM117[a]	National	0.7	0.5	——	80	3.0	0	0	No	8

[a]For test configuration with $C_{in} = 0.1$ μF, and $C_{out} = 2$ μF.

Table 9 Summary of SEE data for PWMs

PWMs/gate drivers						
Device	Vendor	Double/missing pulses	Soft start (SS) duration	Upset rate/year	Transient duration	Latchup (Au, LET = 83.9)
UC1864	Unitrode	Yes/Yes	Varies	0.8	N/A	No
UC1803	Unitrode	Yes/Yes	2–4 ms	0.4	N/A	Damage observed from Cl (LET = 11.1)
UC1825	Unitrode	Yes/Yes	None	2.4×10^{-3}	N/A	No
SG1825	Silicone General	Yes/Yes	None	4.5×10^{-3}	N/A	No
SG1525	Silicone General	No/Yes	None	2.7×10^{-3}	N/A	No
UC1705	Unitrode	N/A	N/A	3.4×10^{-3}	±2.5/150 ns	No

Table 10 Summary of SEU data for frequency synthesizers

Frequency synthesizer circuits[a]				
Device	Vendor	Worst-case impact	Upset rate/year	Latchup (Au, LET = 83.9)
LM2315	National	Permanent change in frequency, command is required to recover	5.9×10^{-9}	No
SP8858	Plessey	Permanent change in frequency, command is required to recover	5.5	No
SP8855	Plessey	Permanent change in frequency, command is required to recover	2.2×10^{-2}	No
3261	Qualcomm	Permanent change in frequency, command is required to recover	1.5	No
3282A	Peregrine	Permanent change in frequency, command is required to recover	3.2×10^{-5}	No

[a]Any spurious frequency change at the synthesizer output was classified as an SEU event.

Table 11 Summary of SEU data for digital and RF devices

Digital							RF Devices						
Device	Vendor	Worst-case positive transient	Worst-case negative transients	Duration, ns	Upset rate/year	Latchup (Au, LET = 83.9)	Device	Vendor	Worst-case Impact	Worst-case transients	Typical transients	Duration	Latchup (Au, LET = 83.9)
54AC2525	National	0.2	0.2	100	6.5×10^{-3}	No	AC936	Cougar	None	None	None	——	No
SN54S30N	Texas Instrument	2.5	2.5	50	2.9×10^{-2}	No	2NE356	NEC	None	None	None	——	No

2) Two types of digital devices that were tested had low SET upset rate ($R < 0.05$ upsets/device/year) and low amplitude (from 0.2 to 2.5 V), and short duration transients (<150 ns).

Conclusions

Test data for a large number of electronic components are presented as part of a methodology to mitigate the effects of SEE on spacecraft performance. More detailed information is presented than has been previously published, specifically, device cross section, worst-case transients, and duration and probability of occurrence as a function of transient amplitude. Although many previous papers presented information on worst-case amplitude and total upset cross section, they did not include the upset rate as a function of the amplitude of the transients. This information, however, is critical in determining the realistic probability of the upset of specific linear-device-based circuits and in making practical decisions about necessity and the type of protective measures, because circuit sensitivity to transients can vary from 200 mV to 15 V depending on the specifics of the design. The probability of the device upsets that result in 5 or 15 V transients is an order of magnitude lower than that for 200-mV transients. Therefore, if total upset rate (upset rate for all transients >200 mV) is used to estimate upset rate for the circuit that is only susceptible to 5-V transients, this will result in gross overestimate of the upset rate. In addition to allowing the design engineer to make sound design tradeoffs, such data allow establishment of a much better correlation between upset rate estimates and actual spacecraft on-orbit performance and improvement of our ability to recognize and troubleshoot on-orbit anomalies.

The data that show the dependence of transient duration and amplitude on the output capacitance for voltage references were not previously available and are of great practical value to the circuit designers. They show, for example, that, although the output capacitance reduces the transient amplitude, it also can extend the duration of the transients by more than an order of magnitude. Therefore, the attempt to reduce the transients with an output capacitor can make matters worse by extending the duration of the transients. Some circuits may be immune to high-level transients of short duration, but will be upset by low-level long-duration transients. The data presented in this paper allow spacecraft designers to tailor their SEE protection by optimizing output capacitance values to best suit their application.

Most important, a large and detailed database that was collected allowed us to develop general design guidelines for a specific class

of devices. These design guidelines can be used by designers to tailor SEE protection for any circuit based on these device types and eliminates or reduces the need for SEE testing for each individual device. These design guidelines have been successfully incorporated into Lockheed Martin Commercial Spacecraft design. Their use minimized the need for costly SEE testing and ensured SEE immune design as demonstrated by excellent on-orbit performance of many components that were designed using the methods and data described in this paper.

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